## REMARKS

Claims 1-27 are pending and rejected. Claims 1, 9, 17, 22, and 25 are amended. No new matter is added.

35 U.S.C. §101

Claims 25-27 are under 35 U.S.C. §101. Claim 25 is amended, and claims 26 and 27 depend from independent claim 25. Accordingly, for at least these reasons, Applicants respectfully request that the Section 101 rejection of claims 25-27 be withdrawn.

First 35 U.S.C. §103 Rejection

Claims 1-2, 5, 17-21, and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Whitten (U.S. Patent No. 5,805,795) in view of Bening ("Optimizing Multiple EDA Tools within the ASIC Design Flow").

Whitten discloses a method and a computer system for selecting a set of test cases for use in testing a target software program having a number of possible code blocks that may be exercised (col. 3, lines 10-15). The computer system also includes a comparator for identifying a set of the test cases that exercises a maximum number of the identified code blocks in a minimum amount of time (col. 3, lines 43-46).

Bening discloses that a designer instantiates selected text macros and actual design variables corresponding to the macro's formal parameters (page 54, left column). A preprocessor replaces the text-macro references with specific module instances and creates a final Verilog register transfer level (RTL) file (Id).

Applicants respectfully submit that neither Whitten nor Bening, considered alone or in combination, disclose or suggest a method as called for by claim 1. For example, the combination of Whitten and Bening does not disclose or suggest "selecting a plurality of submodules from a design module library, wherein a probabilistic function is applied to select the plurality of submodules of different types from the library, wherein said selecting the plurality of submodules is constrained based on a hardware family of the one of the test designs, wherein the hardware family is selected from a plurality of hardware families". Rather, Whitten discloses identifying the set of test cases that tests a maximum number of identified code blocks in a minimum amount of time and Bening discloses replacing the text-macro references with specific module instances. There is no disclosure or suggestion in Whitten and Bening of selecting the plurality of submodules from the design module library by constraining the

selection based on a hardware family of a test design. Hence, for at least these reasons, claim 1 would not have been obvious over the combination of Whitten and Bening.

For at least the same reasons, neither Whitten nor Bening, considered alone or in combination, disclose or suggest a computer system as recited in claim 17 and an apparatus as recited in claim 25. Hence, claims 17 and 25 would not have been obvious over the combination of Whitten and Bening.

The dependent claims, include, by virtue of their dependency, the features of the independent claims on which they are based. As such, the dependent claims would not have been obvious for at least the same reasons as their respective independent claims.

Therefore, for at least the reasons set forth above, Applicants respectfully request that the Section 103 rejection of Claims 1-2, 5, 17-21, and 25-27 be withdrawn.

Second 35 U.S.C. §103 Rejection

Claims 4, 6-13, 15, and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Whitten in view of Bening and in further view of Zaidi (2002/0038401 A1).

Claims 4, 6-13, and 15 depend from independent claim 1 and claims 22-24 depend from independent claim 17. As explained above, the combination of Whitten and Bening does not disclose or suggest a method as recited in claim 1 and does not disclose or suggest a computer system as recited in claim 17. Moreover, Zaidi is not cited to address the deficiencies mentioned above with respect to Whitten and Bening. For example, Zaidi is cited to teach that "instantiation constraints are used to select the plurality of submodules" and "providing logic to interconnect the plurality of parameterized modules comprises identifying inputs and outputs (Office Action, pages 4 and 5). Accordingly, for at least these reasons, claims 4, 6-13, 15, and 22-24 would not have been obvious over the combination of Whitten, Bening, and Zaidi.

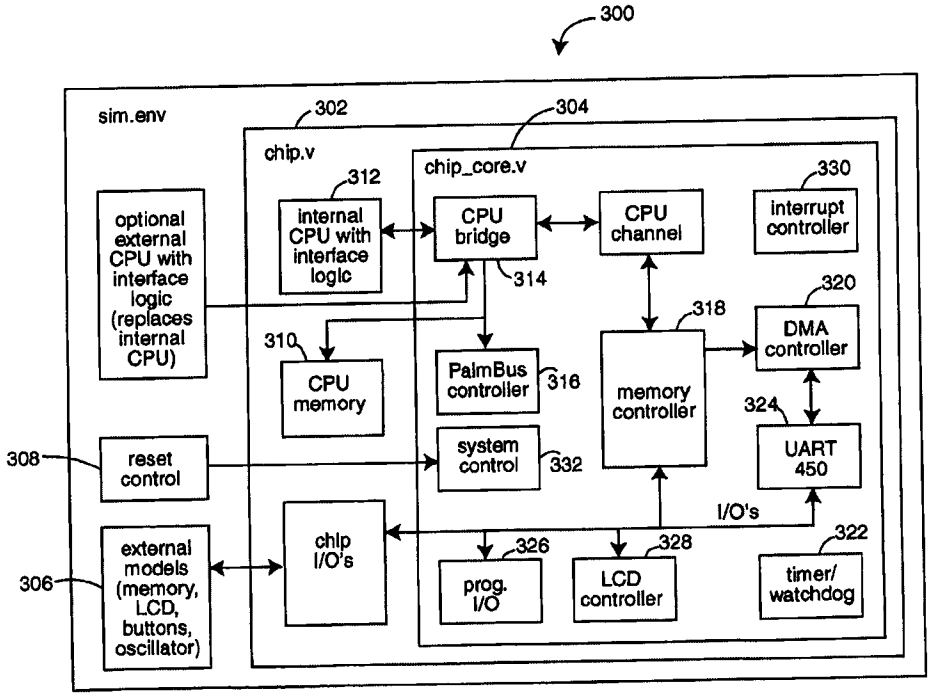
Official Notice – Claim 9

The Office Action admits that the combination of Whitten, Bening, and Zaidi does not teach classifying inputs and outputs as clock lines, control lines, and data lines, but does not provide a specific reference where such a limitation is found, instead arguing that one of ordinary skill in the art would have found it obvious to have this feature to prevent errors when interconnecting inputs and outputs. Applicants hereby traverse the assertion and requests that a reference be cited in support of the position outlined in the Office Action.

Applicants respectfully submit that given the combination of Whitten, Bening, and Zaidi, it would not have been obvious to arrive at the claimed limitation that "providing logic to

interconnect the plurality of parameterized submodules further comprises classifying inputs and outputs as clock lines, control lines, and data lines". Rather, Whitten discloses identifying the set of test cases that tests a maximum number of identified code blocks in a minimum amount of time and Bening discloses replacing the text-macro references with specific module instances. Moreover, Zaidi discloses a simulation environment 300 that is modeled after how a user design might actually appear in a system, either as a single chip on a board or as a subsystem in a larger system-on-chip (paragraph 48). The simulation environment 300 is typically embodied and delivered to a user as a computer data file (Id). The simulation environment 300 is illustrated in Figure 3, reproduced below.

Fig. 3




None of the devices shown in the simulation environment 300 show control lines, data lines, and control lines. Hence, for at least these reasons, the feature of claim 9 would not have been obvious over the combination of Whitten, Bening, and Zaidi. Accordingly, if the Examiner wishes to maintain this assertion, in accordance with MPEP §2144.03, Applicants respectfully requests the Examiner to cite art of record which supports the Examiner's assertion.

Official Notice – Claim 13

The Office Action admits that the combination of Whitten, Bening, and Zaidi does not teach that parameterizing the plurality of submodules comprises defining interfaces, data width,

and the type of signal for input and output lines associated with the submodule, but does not provide a specific reference where such a limitation is found, instead arguing that one of ordinary skill in the art would have found it obvious to have this feature to prevent errors when interconnecting inputs and outputs. Applicants hereby traverse the assertion and requests that a reference be cited in support of the position outlined in the Office Action.

Applicants respectfully submit that given the combination of Whitten, Bening, and Zaidi, it would not have been obvious to arrive at the claimed limitation of "parameterizing the plurality of submodules comprises defining interfaces, data width, and the type of signal for input and output lines associated with the submodule". Rather, Whitten discloses identifying the set of test cases that tests a maximum number of identified code blocks in a minimum amount of time and Bening discloses replacing the text-macro references with specific module instances. Moreover, Zaidi discloses the simulation environment 300 and the environment does not show interfaces, data width, and the type of signal for input and output lines associated with a submodule. Hence, for at least these reasons, the feature of claim 13 would not have been obvious over the combination of Whitten, Bening, and Zaidi.

Accordingly, if the Examiner wishes to maintain this assertion, in accordance with MPEP §2144.03, Applicants respectfully requests the Examiner to cite art of record which supports the Examiner's assertion.

Third 35 U.S.C. §103 Rejection

Claims 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Whitten in view of Bening and in further view of Goossens ("Design of Heterogeneous ICs for Mobile and Personal Communication System").

Claims 14 and 16 depend from independent claim 1. As explained above, the combination of Whitten and Bening does not disclose or suggest a method as recited in claim 1. Moreover, Goossens is not cited to address the deficiencies mentioned above with respect to Whitten and Bening. For example, Goossens is cited to teach "submodules comprising of adders and phase lock loops" and "clock structures that include a plurality of synchronous and asynchronous structures" (Office Action, page 7). Accordingly, for at least these reasons, claims 14 and 16 would not have been obvious over the combination of Whitten, Bening, and Goossens.

Fourth 35 U.S.C. §103 Rejection

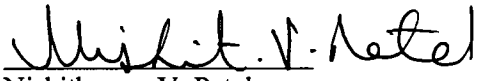
Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Whitten in view of Bening and in further view of Rajsuman (U.S. Patent No. 6,678,645).

Claim 3 depends from independent claim 1. As explained above, the combination of Whitten and Bening does not disclose or suggest a method as recited in claim 1. Moreover, Rajsuman is not cited to address the deficiencies mentioned above with respect to Whitten and Bening. For example, Rajsuman is cited to teach "generating a plurality of test designs of an ASIC including DSP and memory submodules" (Office Action, page 8). Accordingly, for at least these reasons, claim 3 would not have been obvious over the combination of Whitten, Bening, and Rajsuman.

Conclusion

In light of the above remarks, the rejections to the independent claims are believed overcome for at least the reasons noted above. Applicants believe that all pending claims are allowable in their present form. Please feel free to contact the undersigned at the number provided below if there are any questions, concerns, or remaining issues.

Respectfully submitted,



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